B.Tech. (CSE) 4th Semester (G Scheme) Examination, July-2022 COMPUTER ORGANIZATION AND ARCHITECTURE Paper- PCC-CSE-204-G

Time allowed: 3 hours]

[Maximum marks: 75

Note: Attempt any five questions in all. Questions
No. 1 is compulsory.

- 1. (a) What do you mean by term "register transfer"?
 - (b) Convert octal 736.4 to decimal.
 - (c) What is the requirement of common bus System?
 - (d) Discuss Relative Address Mode.
 - (e) What is role of Strobe Control in asynchronous data transfer?
 - (f) Define Write-through and Write-back cache. 6×2.5=15
- 2. (a) Explain Subtraction of Unsigned Numbers in Complement number system with appropriate example.
 - (b) Explain Floating Point Representation in detail.

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3.	(a).	Explain selective set, selective complemen selective clear.	t and
	(b)	List and explain Logic Micro operation details.	ns in 8
4.	(a)	Explain Stored Program Organization in deta	uil. 7
	(b)	Draw and explain input-output configuration basic computer.	n of
		Also explain Input-Output instructions.	8
5.	(a)	Explain four types of instruction formats in de with suitable example.	tails 8
	(b)	Explain various Data Transfer Instruction details with suitable example.	s in
6.	(a)	Discuss four-segment instruction pipeline vidiagram(s).	with 9
	(b)	How the throughput of a system can be enhan with parallel mechanisms?	ced
7.	(a)	Explain Flynn's classification of Computers details.	s in
	(b)	Explain Asynchronous data transfer w Handshaking method.	ith 7

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	8. (a)	What is priority interrupt? Explain Daisy Chaining in details
ı	(b)	Write a detailed note on Direct Memory Access (DMA).
f	9. (a)	What do you mean by cache memory? Draw and explain the block diagram of cache Memory. Discuss associative mapping in organization of

What do you mean by address space and memory (b) space in virtual memory? Also explain the relation between address space and memory space invirtual memory.

organization of cache memory.

cache memory. Discuss direct mapping in

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