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B. Tech. (CSE) 3rd Semester
Examination – February, 2022

DIGITAL ELECTRONICS

Paper : PCC-CSE-205-G

Time : Three Hours]　　　　　　　　[Maximum Marks : 75

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt *five* questions in all, selecting *one* question from each Unit. Question Number **1** is *compulsory*. All questions carry equal marks.

1. Write note on the following :　　　　　$5 \times 3 = 15$

   (a) What do you mean by Latch ?

   (b) What is race-around condition ?

   (c) Define CAM.

(d) Explain Encoders.

(e) Differentiate Decoder and Demultiplexer.

UNIT – I

2. (a) Discuss error detection and correction code in detail.   7.5

(b) Realize $Y = \overline{A + B + C + D}$ using 2 input NOR gate only.   7.5

3. (a) Design EX-OR and EX-NOR using universal gates.   7.5

(b) Prove A + BC = (A + B) (A + C).   7.5

UNIT – II

4. Find out the minimal SOP expression using K-Map method :   15

$$Y(A, B, C, D) = \Pi M(2, 3, 5, 9, 11, 13) . d(1, 7, 12, 15)$$

5. (a) Design 8 : 1 multiplexer using 4 : 1 multiplexer only.   7.5

(b) Justify full subtractor is a combination of two half subtractor.   7.5

UNIT – III

6. (a) Convert SR flip-flop to JK flip-flop.   7.5

    (b) Design mod-7 up asynchronous counter.   7.5

7. (a) How ring counter works ? Explain.   7.5

    (b) Explain the working of master slave JK flip-flop.

     7.5

UNIT – IV

8. What are the specifications of A/D converters ? Also explain the working of Dual slope A/D converter with diagram.   15

9. Write short note on : $2 \times 7.5 = 15$

    (i) RAM and ROM

    (ii) PAL and PLA

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