Roll No. .....

24487

B. Tech. 7th Semester (CSE)
(Common with Special Chance)
Examination – December, 2019

ADVANCED COMPUTER ARCHITECTURE

Paper : CSE-401-F

Time : Three Hours] *[Maximum Marks : 100*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt any ***five*** questions, selecting ***one*** question from each Section. Question Number **1** is ***compulsory.*** All questions carry equal marks.

1. (a) What are Horizontal and Vertical Microinstruction ? Write their Instruction formats.

(b) What is Cache Coherence ? Explain in detail.

(c) Explain Rau's Model.

(d) What is Hazard in Pipeline ? Explain its types.

SECTION – A

2. Explain Virtual to Real Mapping and Instruction Timing in detail.

3. Explain Instructions Sets with application area and also focus on the processor Evaluation Matrix.

SECTION – B

4. Write different policies strategies for line replacement at miss time in detail.

5. Explain T Cycle and also discuss overlapping the T cycle in V-R translation.

SECTION – C

6. Give a brief discussion on Processor Memory Modeling using Queuing Theory.

7. What are Open, Closed and Mixed Queue Models ? Also focus on waiting time, performance and buffer size.

SECTION – D

8. Explain Vector Processors and Vector Memory in detail.

9. What is Shared Memory Multiprocessor ? Explain its types. Discuss synchronization and coherency in Shared Memory Multiprocessors.
