Roll No. .....

3095

B. Tech. 4th Semester (EE) Examination – July, 2021

DIGITAL ELECTRONICS

Paper : PCC-EE-202-G

Time : Three hours] *[Maximum Marks : 75*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Question No. **1** is ***compulsory***. Attempt ***four*** more questions, selecting ***one*** question from each Section.

1. (a) De-Morganize the following function $[(A + B') + (C + D')]'$. $1.5 \times 10 = 15$

(b) Represent $(32)_{10}$ in excess 3 code.

(c) Realize AND gate using NAND.

(d) Define encoder.

(e) What is the Gray equivalent of$(25)_{10}$.

(f) What is programmable logic array ? How it is differs from ROM ?

(g) How many address bits are required to represent a 4 K memory ?

(h) For JK flip-flop if, J = 0, K = 1, what will be the output after clock pulse ?

(i) How many two input AND gates and two input OR gates are required to realize $Y = BD + CE + AB$?

(j) Write the decimal equivalent of hex number 1 A53

SECTION – A

2. (a) Give comparison between various logic families. 10

(b) Draw and give truth table of following gates : 5

(a) EX-OR

(b) AND

(c) OR

(d) NOR

(e) NAND

3. (a) Write in detail about various error detecting and correction codes. 10

(b) Using Boolean algebra, reduce the following functions : 5

(i) $y = A\overline{B}C + B\overline{D} + AB\overline{D} + \overline{A}C$

(ii) $y = [(A + B)(\overline{A} + B)] + [(A + B)(A + \overline{B})]$

SECTION – B

4. (a) What is half adder ? Explain a half adder with the help of truth table and logic diagram. 10

(b) Use K-map to simplify each expression : 5

$$Y = (AC + A\overline{C}D)(AD + AC + BC)$$

5. (a) What is De-multiplexer ? Explain, with the help of suitable block diagram and logic circuit of 1 to 16 de-multiplexer. 10

(b) Implement the function $F(x, y, z) = \Sigma(1, 2, 6, 7)$ using 4×1 multiplexer. 5

SECTION – C

6. (a) What is synchronous counter ? Design a MOD-5 synchronous counter using J-K flip flop. 10

(b) Explain working of serial in serial out shift register. 5

7. (a) Draw the circuit diagram of Master Slave J-K flip flop using NAND gates. What is the race around condition ? How is it eliminated in a Master slave J-K flip flop ? 10

(b) What is shift register ? What are its various types ? List out some applications of shift register. 5

SECTION – D

8. With the help of R-2R binary ladder, explain the working of 4-bit D/A converter. 15

9. Differentiate between following : 15

(i) Static and dynamic RAM

(ii) PLA and PAL

(iii) RAM and ROM

B.Tech. (EE) 4th Semester (G-Scheme)
Examination, July–2022
DIGITAL ELECTRONICS
Paper– PCC-(EE-202-G)

Time allowed : 3 hours] *[Maximum marks : 75*

Note : *Attempt **five** questions in total selecting **one** from each unit. **Question number 1 is compulsory.***

1. (a) Find the decimal equivalent of the following binary numbers assuming sign magnitude representation of binary numbers 6×2.5

(i) 101100 (ii) 1111

(b) Represent the following numbers in one's compliment form

(i) 11010100 (ii) 10010100

(c) Find two's compliment of the numbers

(i) 01100100 (iii) 11011000

(d) Explain half subtractor.

(e) What do you mean by Don't care condition?

(f) Explain D-type flip-flop.

Unit - I

2. Explain operation of Schottky TTL. 15

3. Formulate 8-bit ASCII code for 'My dear Surender' and represent it in hexadecimal code with (i) Even parity (ii) Odd parity

Unit - II

4. Minimise the logic function in POS form as: 15

$f(A, B, C, D) = \Pi M (4, 6, 10, 12, 13, 15)$

5. Simplify the Logic function 15

$Y(A,B, C, D) = \Sigma M(0, 1, 3, 7, 8, 10, 11, 15)$

Using the Quine - McCluskey minimization technique.

Unit - III

6. (a) Explain parallel to serial converter. 7

(b) What are the applications of converters. 8

7. Explain clocked S-R Flip-Flop. 15

Unit - IV

8. (a) Explain successive approximation A/D converter. 10

(b) What do you man by CAM. 10

9. (a) Explain parallel comparator A/D converter. 10

(b) Discuss programmable array logic. 5