Roll No. .....

3092

B. Tech. 4th Semester (ECE) Examination – May, 2023

DIGITAL ELECTRONICS

Paper : PCC-ECE-205G

Time : Three hours] *[Maximum Marks : 75*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt ***five*** questions in all, selecting ***one*** question from each Unit. Question No. 1 is ***compulsory***. All questions carry equal marks.

1. (a) Convert : $3 \times 5 = 15$

   (i) Decimal 109.25 into binary

   (ii) Hex 2AD6 into Octal

   (b) Difference between combinational and sequential circuits.

   (c) Difference between latch and flip flop.

   (d) Write briefly about PAL.

   (e) List out components of ASM charts.

P. T. O.

UNIT – I

2. (a) Discuss addition and subtraction of two numbers (78 and 55) using complements of them. 7

(b) Solve the followings : $2 \times 4 = 8$

(i) $A + BC + (CA - ABC)(A - B - C)$

(ii) $(A + C + B - 1) + (AB + 1)(B + C + 1)$

3. (a) Simplify the function using Quine McClusky method : 10

$X(A, B, C, D) = m\Sigma(0, 1, 2, 5, 9, 11, 12, 14)$

(b) Give out the sequence of steps to solve a problem using K-map method. 5

UNIT – II

4. (a) At the receiver the Hamming code data received is 10111010111. Find out the error and also give the correct code. The even parity has been used at transmitter. 10

(b) How De-multiplexer differ from decoders ? Can they be used for each other ? 5

5. (a) Design a binary synchronous counter which counts upto 9 and then starts reverse counting upto zero i.e. initial stage and repeats the process. 8

(b) Design decimal to hexadecimal encoder. Also give out TT. 7

UNIT – III

6. Write short notes on the followings : $2 \times 7.5 = 15$

(a) Design of D and T type flip flop using SR flip flop

(b) Up Down counters

7. (a) Discuss working of ripple counters. 8

(b) Design a mode 10 counter. 7

UNIT – IV

8. (a) Discuss briefly designing and working of PAL. 8

(b) Discuss in details the design procedure for asynchronous logic circuits. 7

9. Write briefly about the followings : $3 \times 5 = 15$

(a) RAM

(b) ASM design

(c) ROM

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B. Tech. 4th Semester (ECE) Examination – July, 2021

DIGITAL ELECTRONICS

Paper : PCC-ECE-205-G

Time : Three hours] *[Maximum Marks : 75*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Question No. **1** is ***compulsory***. Attempt any ***one*** from each Section.

1. (a) Find the hex sum of $(93)_{16} + (DE)_{16}$. $2.5 \times 6 = 15$

(b) Differentiate between latch and flip flop.

(c) Why NAND-NAND realization is preferred over AND-OR realization ?

(d) What is Race around condition ?

(e) Realize OR gate using universal gates.

(f) What is programmable logic array ? How it is differs from ROM ?

SECTION – A

2. (a) Reduce by K-mapping and implement using NOR-NOR logic : 10

$$y = \sum m\,(1,2,3,4,6,7,10,11,13,14)$$

(b) Find 9's complement and 10's complement of 155 and 255. 5

3. (a) State and prove De-Morgan's theorem 5

(b) What is Quine McCluskey method ? Use QM method to reduce each following expression to a minimum SOP form : 10

(i) $y = \overline{ABCD} + \overline{ABC}D + ABCD + ABC\overline{D}$

(ii) $y = \overline{AB}(\overline{CD} + \overline{C}D) + AB(\overline{CD} + \overline{C}D) + A\overline{BC}D$

SECTION – B

4. (a) Perform each of the following conversions : 10

(i) $(11010)_2 = (\ )_{BCD}$

(ii) $(10111011)_2$ into its equivalent grey code.

(b) Determine the single error correcting code for the information code 10111 for odd parity. 5

5. (a) Implement the function $F(x, y, z) = \Sigma(1, 2, 6, 7)$ using 4×1 Multiplexer. 10

(b) Explain full adder circuit in detail. 5

SECTION – C

6. (a) Convert the following : 10

   (i) SR Flip flop into JK Flip flop

   (ii) JK Flip flop into D Flip flop

   (b) Write short note on Edge triggered Flip flop. 5

7. (a) Explain working of serial in serial out shift register. 10

   (b) Design MOD-10 synchronous counter with JK-Flip flop. 5

SECTION – D

8. What is FSM ? Describe types of FSM. Mention advantages, disadvantages and applications for the same. 15

9. Compare PAL and PLA. Also draw combinational circuit for a PLA with three inputs, three product terms and two outputs. 15

B.Tech. (ECE) 4th Semester (G-Scheme)
Examination, July–2022
DIGITAL ELECTRONICS
Paper– PCC-ECE-205-G

Time allowed : 3 hours] *[Maximum marks : 75*

Note : ***Question no. 1 is compulsory****. Attempt* ***one*** *questions from each unit.*

1. (a) What are the differences between Combinational Circuits and Sequential Circuits? 2.5

   (b) What are the applications of Demultiplexer? 2.5

   (c) What is the difference between Synchronous and Asynchronous Counters? 2.5

   (d) What are the applications of Flip-Flops? 2.5

   (e) What is Half-Adder? 2.5

   (f) What are the limitations of the Karnaugh Map? 2.5

Unit - I

2. Find a minimal SOP representation for f (A,B,C,D,E) = Σm(1,4,6,10,20,22,24,26) + d(0,11,16,27) using K-map method. Draw the circuit of the minimal expression using only NAND. 15

3. (a) List out the basic rules (laws) that are used in Boolean algebra expressions with example. 8

(b) Implement the expression Y (A, B, C) = ΠM (0, 2,4,5,6,) using only NOR-NOR logic. 7

Unit - II

4. (a) Draw the block schematic of Magnitude comparator and explain its operation. 8

(b) Draw & explain the block diagram of a 4-bit parallel Adder / Subtractor. 7

5. (a) Design & explain the working of Gray to BCD converter. 8

(b) Explain even parity checker and generator. 7

Unit - III

6. (a) Design and explain the working of an 4-bit Parallel counter. 8

(b) Design and explain the working of a BCD ripple counter with timing diagram. 7

7. (a) Explain the operation of universal shift register with neat block diagram. 8

(b) Explain the working of Master/Slave JK FF. 7

Unit - IV

8. (a) Write a note on FPGA with neat diagram. 8

(b) Write short notes on PLD, types of PLDs. 7

9. Design a clocked sequential machine using JK flip flops for the state diagram shown in figure. Use state reduction if possible and make proper state assignment. 15