Roll No.

3326

B. Tech. 6th Semester (ECE) Examination – May, 2023 CMOS DESIGN

Paper : PCC-ECE-308-G

Time : Three Hours]

[Maximum Marks : 75

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

- *Note* : Attempt *five* questions in all, selecting *one* question from each Unit. Question No. 1 is *compulsory*. All questions carry equal marks.
- **1**. Explain the following :

 $2.5 \times 6 = 15$

- (a) Stick diagram
- (b) Compare NMOS and PMOS transistor
- (c) Sketch the transmission gate or pass gate
- (d) MOSFET
- (e) Latch
- (f) CMOS

3326-1200-(P-3)(Q-9)(23)

P. T. O.

UNIT – I

ÿ

:		 i) Illustrate ideal I-V characteristics of M transistors with necessary diagrams. Equation BC datasy model 	MOS 8
		 Explain RC delay model. 	7
3	t. W fo	rite short notes and draw stick diagram on llowing :	the
	(a)) CMOS Inverter	7
	(b)) NAND Gate	8
			0
UNIT – II			
4.	(a)	Compare the static CMOS inverter Pseudo-nMOS inverters.	and 8
	(b)	Explain about the dynamic cascode voltage sw logic with neat diagram.	itch 7
5.	(a)	Explain the following dynamic circuits.	8
		(i) Domino logic	
		(ii) Dual-rail Domino logic	
	(b)	Classify the various Static CMOS circuits combinational circuits.	for 7
UNIT – III			
6.	(a)	Discuss in detail about various pipelini techniques and explain in detail.	ing 7
	(b)		8
7.	(a)	Write about Schmitt trigger and its properties.	8
	(b)	What is Astable sequential circuits.	7
326			

3326- -(P-3)(Q-9)(23) (2)

UNIT - IV

8. Explain the following : 15(i) Shifters

(ii) ALUs

9. (a) Design a one transistor DRAM cell. **7**

.

(b) Draw and explain the architecture of large memory array. 8